ELIZADE UNIVERSITY, ILARA-MOKIN, ONDO STATE

FACULTY OF ENGINEERING

DEPARTMENT OF COMPUTER ENGINEERING

FIRST SEMESTER EXAMINATION, 2020/2021 ACADEMIC SESSION

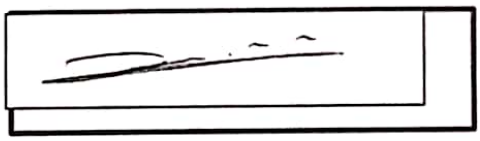
COURSE TITLE: DIGITAL SYSTEM DESIGN WITH VHDL **2 UNITS**

COURSE CODE: ECE 521

EXAMINATION DATE: MARCH, 2021

COURSE LECTURER: PROF AYODEJI O. OLUWATOPE

ENGR. OYEYEMI OYEWOLE



HOD's SIGNATURE

TIME ALLOWED: 2 HOURS 30 MINUTES

INSTRUCTIONS:

1. ANSWER QUESTION **ONE** AND ANY OTHER THREE QUESTIONS
2. SEVERE PENALTIES APPLY FOR MISCONDUCT, CHEATING, POSSESSION OF UNAUTHORIZED MATERIALS DURING EXAM.
3. YOU ARE **NOT** ALLOWED TO BORROW ANY WRITING MATERIALS DURING THE EXAMINATION

QUESTION #1 (COMPULSORY)

A. Use VHDL to design a digital controller for a washing machine which is able to wash, rinse and spin clothes. The state machine sequence is

Idle → wash_fill →wash_agitate → wash_spin → rinse_fill → rinse_agitate → rinse_spin →idle

States interpretation:

Idle *– machine idling;* ***wash_fill*** *– machine fills wash bowl with water;* ***wash_agitate*** *– washing with detergent in progress;* ***wash_spin*** *– detergent draining;* ***rinse_fill*** *– machine fills wash bowl with water for rinse;* ***rinse_agitate*** *– machine rinses clothes with water;* ***rinse_spin*** *– machine drains rinse water and spin clothes to dry.*

Your design should permit **hot wash to wash** and **cold water to rinse. (Hint: add output bits to control water values).** [15 marks]

QUESTION #2

A. Write a VHDL module implementing a 4 input multiplexer. Each input should be a 32 bit wide. [5 marks]

B. Design a three-bit counter using the truth table given in figure 1.0. The codes ABC and $A^+B^+C^+$ represent the current and the next counts respectively. You are required to show your algebraic equations, minimization processes, and the realized logic circuits. [10 marks]

ABC	$A^+B^+C^+$
000	001
001	010
010	011
011	100
100	101
101	110
110	111
111	000

Figure 1.0: Three-bit Counter Truth Table

QUESTION #3

A. Design a 4-bit full adder and also write the VHDL code. [5 marks]

B. Use VHDL to implement the traffic light signals depicted in figures 2 & 3. [10 marks]

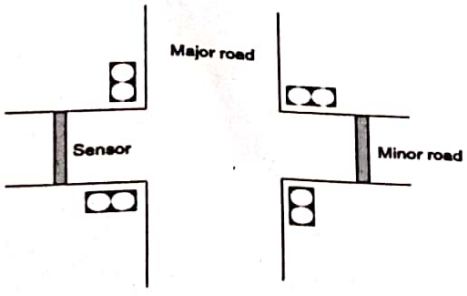


Figure 2: Traffic Signal

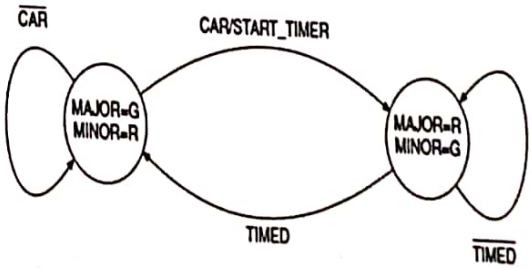


Figure 3: State Machine for Traffic Signal Controller

QUESTION #4

A. Draw the circuit diagram that implements the expression $x = \overline{A}BC(\overline{A+D})$ using logic gates with no more than three inputs. Draw its waveform graphs [5marks]

B. With examples, differentiate between a sequential circuit and combinational circuit. [10 marks]

QUESTION #5

Consider the 4-bit full adder modules in figure 4, using **component instantiation** approach, write a VHDL program to implement the modules [15 marks]

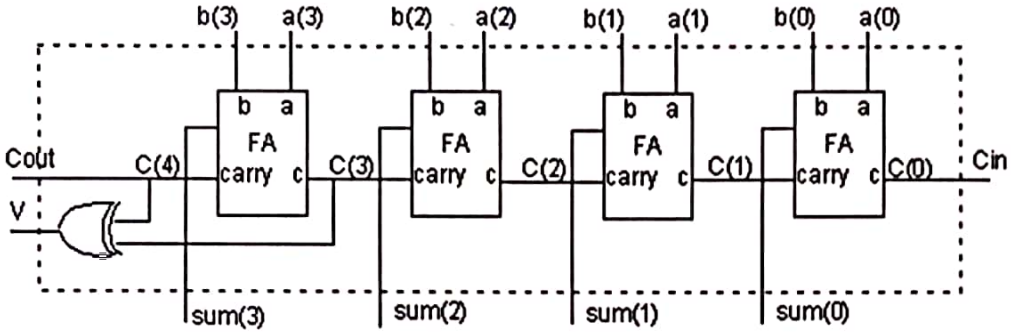


Figure 4: 4-bit adder consisting of full adder modules.

QUESTION #6

A. Design the simplest circuit that has four inputs, x_1,x_2, x_3, and x_4, which produces an output value of 1 whenever three or more of the input variables have the value 1; otherwise, the output has to be 0. [5 marks]

B. Design a VHDL code to implement the parity checker whose state machine is depicted in figure 5. The parity checker should be realised as a sequential circuit. [10 marks]

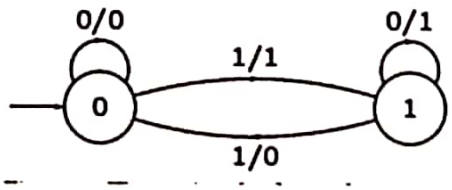


Figure 5: State Machine for a One-bit Parity Checker.